Tools Of The Trade

EMC Design Checklist

Signal Termination

- RC Terminations (33 ohms + 27 pF) on periodic signals
- Group high frequency sources together; minimize trace runs of high frequency signals
- Don't source/sink I/O (whether internal or external) through high frequency devices
- Position oscillators and crystals away from I/O and openings in the chassis
- Snub switching power supply waveforms to minimize High Frequency energy

Decoupling & Power Distribution

- Connect all ground pins of high frequency circuits together
- Maintain 0V reference (bond 0V to chassis)
- Solid power and Ground planes
- Do not insert impedances into Vcc/power traces.

Bonding Checklist

- Bond 0V to chassis ground
- Bond 0V to connector frames and shells
- Bond connector frames to chassis
- Bond metal frames together

Filtering

- Filters are installed at enclosure wall
- LC filter on unshielded cables
- Plan for capacitor on shielded lines

Cabling

- Route cables to avoid coupling
- Use only fully-shielded cables
- Fully-terminate shield grounds to metal/metalized connector shells
- Terminate shells to chassis

Shielding

- The Business Card Test

Suppressors

- Use correctly-rated suppressor line-to-line and line-to-ground
- Gas Tubes
- Varistors
- SAD (Silicon Avalanche Diodes)

In response to regular requests for information from our customers on the fundamentals about EMC and safety compliance, we have assembled a series of information brochures. These brochures are intended to aid design engineering professionals with the basics in many areas; from design features to international compliance to terminology, we intend to cover them all. To receive other brochures in the series or for more information give us a call at 1-800-838-1649.

Running the EMC Gauntlet:

The 10 Basic Steps to Successful EMC Design

Part One: Steps One to Five Abstract

Since the adoption of the FCC Rules and Regulations in 1983, the technological changes that have occurred in the digital device and electronic industry have been unprecedented. From the pokey clock speeds of 4.7 MHz of the original PCs to 400 MHz multi-processor systems, the past fifteen years have witnessed the grand achievements in silicon, components and systems. Ten years ago, most emissions problems were below 200 MHz. As system and clock speeds broke the 25, 33, and 80 MHz marks and testing above 1 GHz is now commonplace.

What haven't changed are the fundamental design features necessary to achieve Electromagnetic Compatibility (EMC). However, many fundamental mistakes are still routinely made. Most of the reasons for equipment failure during EMC testing can be traced to something less than a dozen common, predictable and preventable design flaws. Most designers can improve their EMC performance by observing relatively uncomplicated design guidelines.

The guidelines are distilled into a simple checklist that can be referred to during the design and development of your product. Three areas of concern are paramount:

Circuit boards: the ultimate source or victim in EMC failures. Noise originates and ultimately may affect the circuit board. Source control is the principal issue with reducing emissions and I/O design is the principal issue affecting noise immunity.

Cables: the primary culprit in EMC failures. It is important must learn to live with, accommodate and address the deleterious effects of plugging cables into our electronic creations.

Enclosures: the secondary culprit in EMC failures. Most good designs work the EMC problem first at the printed circuit board level and secondarily at the enclosure level. Doing the job properly at each level means bigger margins, better performance and less delays in the certification process.

I. Introduction of the 0V Noise Return

Kirchoff's law states that currents flow in closed paths. Hence, noise currents flow in closed paths. When tackling emissions or immunity problems, part of the problem is understanding how these currents flow. Controlling the current gives you control of the noise.

Thus, it is necessary to envision in any design, the noise current path. For emissions situations, where the source of the noise is internal to the equipment, it is important to realize that the noise source has a "reference" point. That reference is the 0V pin or node of the noise source.

Consider the following drawing of a noise source, driving currents from one area of the system to another. This source is unintentional; it represents one of many types of noise sources, for example, clock or digital signal harmonics, switched mode power supply emissions, etc.

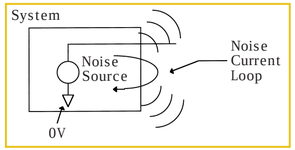


Figure. 0V Noise Reference Return for Emission

Our success depends on returning the noise currents to that point in as direct and efficient way possible. The ultimate performance of shields and filters depends on providing a good, low impedance path to the 0V Reference.

Thus, the first order of business is to provide as much conductor as possible in the system. This conductor is ideally a plane (such as the ground plane on a circuit board) and the best configuration is to connect that plane in multiple places to a metal plate (that can form a portion of the enclosure). The metal plate is in parallel with the circuit board ground plane and lowers the impedance substantially.

Make the most of the metal at hand by making sure that metallic parts are bonded together (bonded meaning well-connected) at mating surfaces. The optimal arrangement is a fully-shielded box that is completely sealed at all seams. The "best" bond is made by overlapping metal parts as much as possible.

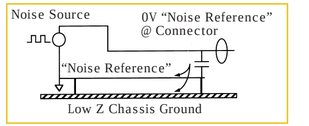
II. Tend to the cables.

Eighty percent of EMC problems involve cables. The objective of shielded cables is to contain and restrain RF noise currents. Shielded cables: Using shielded cables is all but assumed on many high speed systems. A majority of systems require one or more communications or control ports to effect their function. The essentials boil down to is the following:

Use only fully-shielded cables. Acceptable performance can be obtained with a foil-type shield (like an aluminized mylar); the problem with this type of very common shield is the trouble with termination ("grounding") of the shield. Better performance can be obtained with a braid-covered foil shield. This construction lowers the impedance of the shied and, more critically, improves the shield termination. More exotic materials, such as conductive fabrics, are beginning to appear, which also look attractive.

Don't ground with pigtails. The pigtail is a lousy ground at high frequencies—the reason being that the drain wire that is used for the pigtail is really an inductor in disguise—and the inductance is a high impedance at high frequencies. The shield must bond fully (all the way around the shield) to the connector.

On the equipment, the metal connector on the cable must complete the grounding of the cable shield. Scrape or mask off any paint between the metal connector and the chassis to bound the connector. At the board level, the connector shell must be bonded to the 0V reference of the system (chassis + 0V circuit board plane).



Signal control: stopping noise at its source

Source control is a fundamental building block of good EMC design. The effect of the sub-micron features in silicon is to allow systems to scoot along at a crisp 200+ MHz. The downside is that these energetic circuits create harmonics out beyond the 1 GHz frequency range. However, a good majority of systems used in commercial and industrial products (controllers, applicances, etc.) use clock signals below 50 MHz. These zippy gates, which have transition times of less than 1 ns, are overkill for 25 and 33 MHz clock systems. As the processes for making these new silicon brews become more commonplace, it is becomming impossible—or at the least, very difficult—to obtain "slow" logic technologies for driver circuits.

What's a designer to do? For repetitive signals, terminations are recommended. From experience, the most useful, widely applicable and simple termination is shown below:

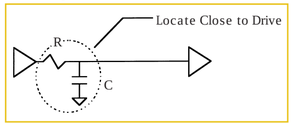


Figure. Default Termination Scheme

This structure provides several benefits: 1) the series resistor tends to "match" the transmission line and reduces the drive current; and 2) the capacitor rolls off high frequency energy due to transitions. The "rule of thumb" is to provide a series 33 ohm resistor with a 27 pF capacitor. The main benefit of having these parts is that a "placeholder" is available after the board is fabricated for tweaking during testing.

The following repetitive signals are candidates for the default termination scheme.

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- Clocks
- Strobes
- Address Latch Enable
- Lower order address and data bits (Ao, A1, A_2, Do, D1, D2)).
- And any other signal that operates in a periodic or semi-periodic fashion.

II. IV. Layout of components, routing of signals and circuit sectoring

By far the cheapest method of noise control involves prudent attention to the location of components in the design. No additional parts costs are incurred in a well-laid out circuit board or a properly configured subsystem or assembly.

The goal is to segregate the circuits into a logical order that minimizes coupling between high frequency circuits, I/O and outside world.

The segregation works for both emissions and immunity. The short list of critical circuits is as follows:

Isolation between the high frequency/high sensitivity circuits and the interconnections minimizes coupling that can lead to an interference problem.

- To minimize noise from exiting the system, the high speed clock distribution and repetetive signals, along with the components that are associated with them, are buried inside the system layout. These networks are grouped tightly together and are routed in the most direct manner possible.
- Next on the list are the address and data busses. These, and the parts associated with them, are placed away from interconnections, headers, etc.

- Critical control circuits (such as reset lines) are routed next. The intent is to isolate these circuits from external noise (such as Electrostatic Discharge).
- Following the critical control circuits, the I/O components are placed next, such as driver/receiver circuits, instrumentation inputs, and other related functions.
- Finally, the filters are located at the connector.

III. Power Distribution

One of the areas of great confusion is in the area of power distribution. Much myth surrounds this area, and many of the discussions of power distribution are overdone and overly complicated.

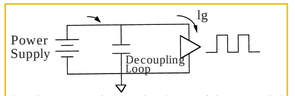
A particularly troublesome evolution is the concept of "isolated" power and ground plane segment used in the construction of circuit boards. This practice uses divided areas of the ground and/or power planes in a circuit to, allegedly, minimize the flow of noisy currents from one area of the power distribution system to the other. This practice started to show up in the early 1980s and has continued to propagate throughout the industry, becoming a standard practice (although malpractice might be a better term).

The reason that the practice doesn't work is that the practice runs afoul of the physics of current flow at radio frequencies.

To illustrate, consider the following circuit—a typical clock/driver arrangement. The clock is humming along at some high frequency, with the edges and transitions of the clock pulse producing high frequency harmonics. To drive this signal, it is necessary to source current from the power distribution rails.

Now, when the gate is switched a flow of

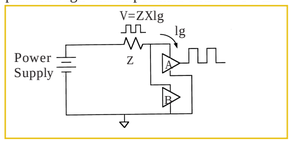
current is initiated from the power plane. This flow of current depletes the electrons in the immediate vicinity of the power connection to the chip and additional electrons move in to restore the charge balance. Decoupling capacitors serve to supply charge. The objective is to supply as much current as possible to the switching gate. The impedance of the plane must be as low an impedance as possible.



Gate draws current from supply rail; most of charge provided by local Vcc plane and from decoupling capacitor. *Ideal case is to provide ALL switching current locally.*

The problems occur when the plane is cut and some impedance is inserted in series with the plane. Sometimes a ferrite bead is used, sometimes an inductor is used and sometimes the plane is reduced to a small interconnect trace.

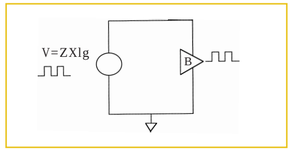
But, as the current flows in to resupply the electrons depleted locally, this current must pass through this impedance and V = I x Z.



Thus, a noise voltage is developed across this impedance. A high frequency, noise voltage that will have the same spectral content as the switched gate.

Now, consider that there are other circuits connected to the isolated power plane. What occurs is that all of these circuits have this

noise voltage "impressed" upon them (basically in series with th rail voltage) and the noise rides on the signals associated with this isolated are.



Now, one area where the argument for separation of is in systems that use true analog circuits. A true analog circuit is one in the traditional sense and has the following attributes: 1) low frequency operation (less than, say 10 kHz); 2) low signal levels (milli-volts, or thereabouts); and 3) operational amplifiers, instrumentation amplifiers and other traditional analog circuits. Even in this case, it is possible to maintain a single ground plane for the system, if good physical layout techniques are applied.

The entire checklist is shown on the inside front cover. In part two we will cover the remaining areas of concern, namely:

- Grounding techniques at connectors and interfaces
- Sealing the enclosure
- Dealing with analog circuits
- Switched mode power supplies

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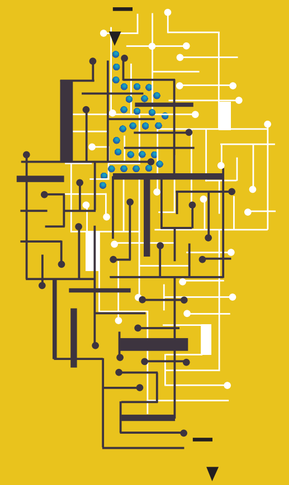

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